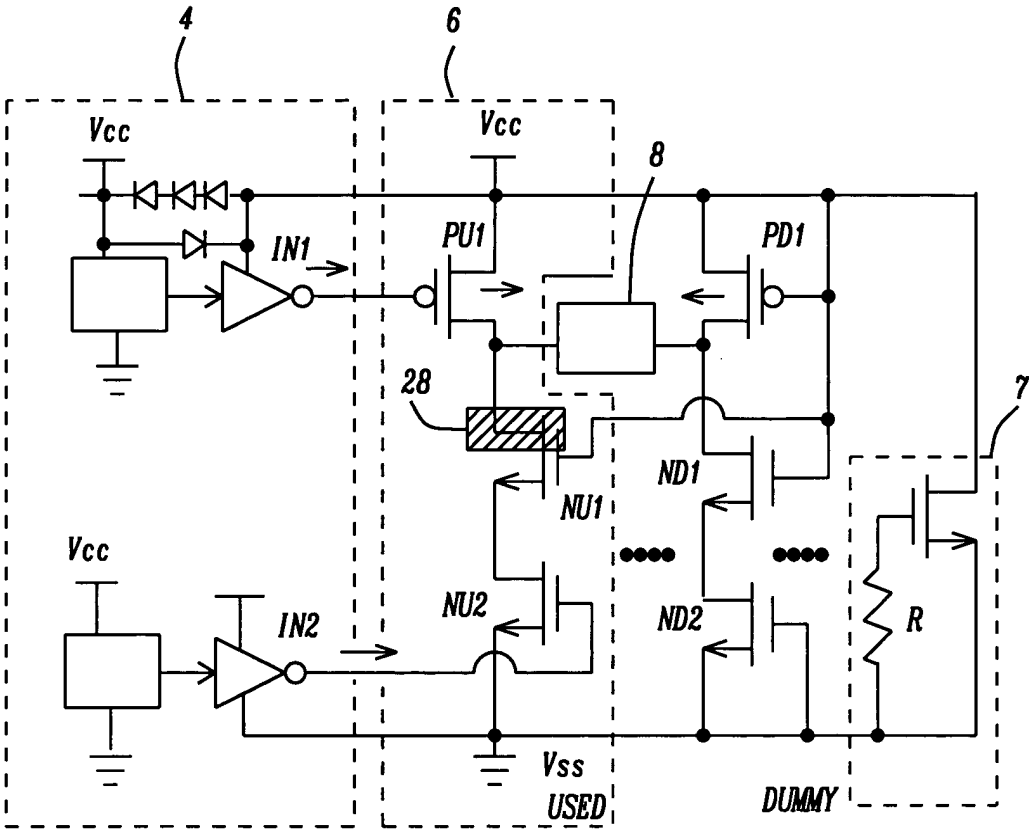


FIG. 1A – Prior Art

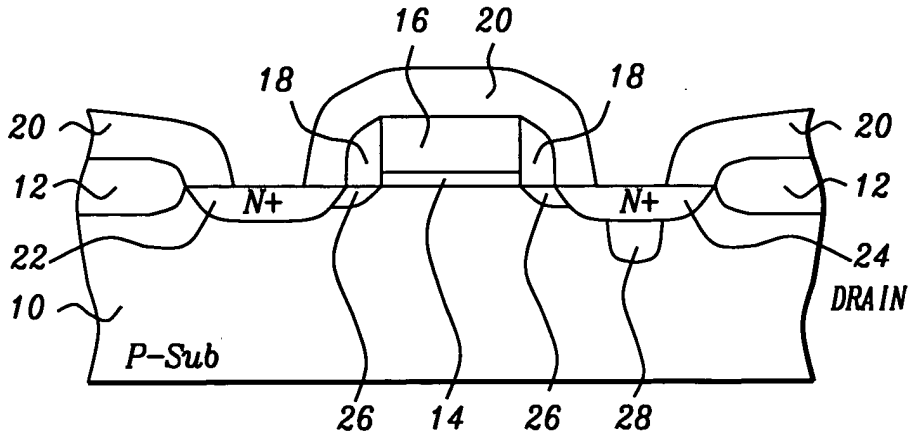


FIG. 1B – Prior Art

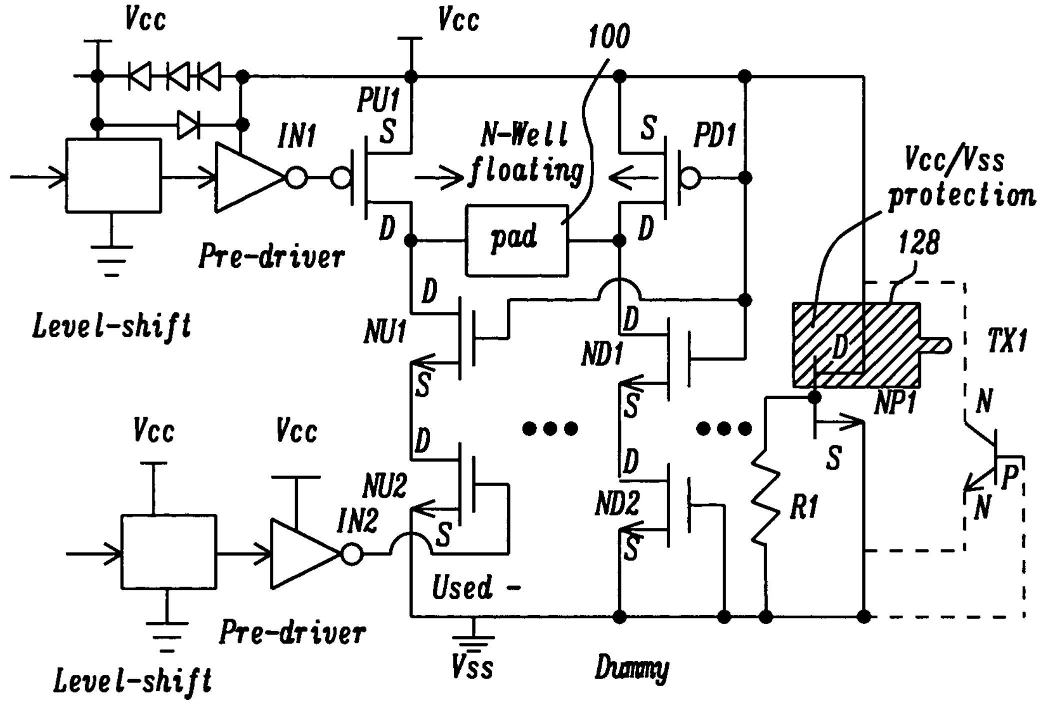

Vcc
Vcc
100
PU1
S
IN1
N-Well
floating
S
PD1
Vcc/Vss
protection
D
pad
D
128
Pre-driver
D
Level-shift
NU1
D
ND1
D
TX1
S
S
NP1
N
D
D
S
Vcc
Vcc
NU2
ND2
R1
P
IN2
S
N
S
Used -
Level-shift
Pre-driver
Vss
Dummy

FIG. 2A

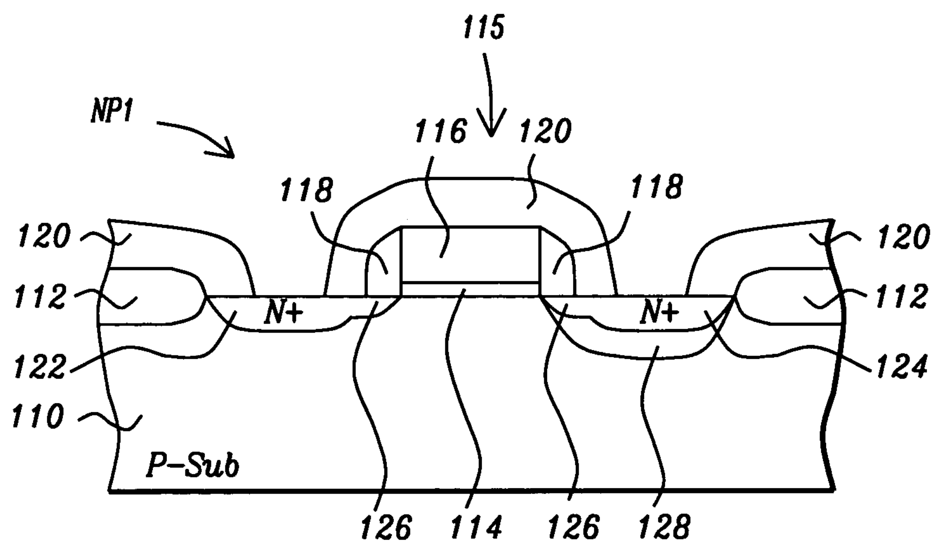
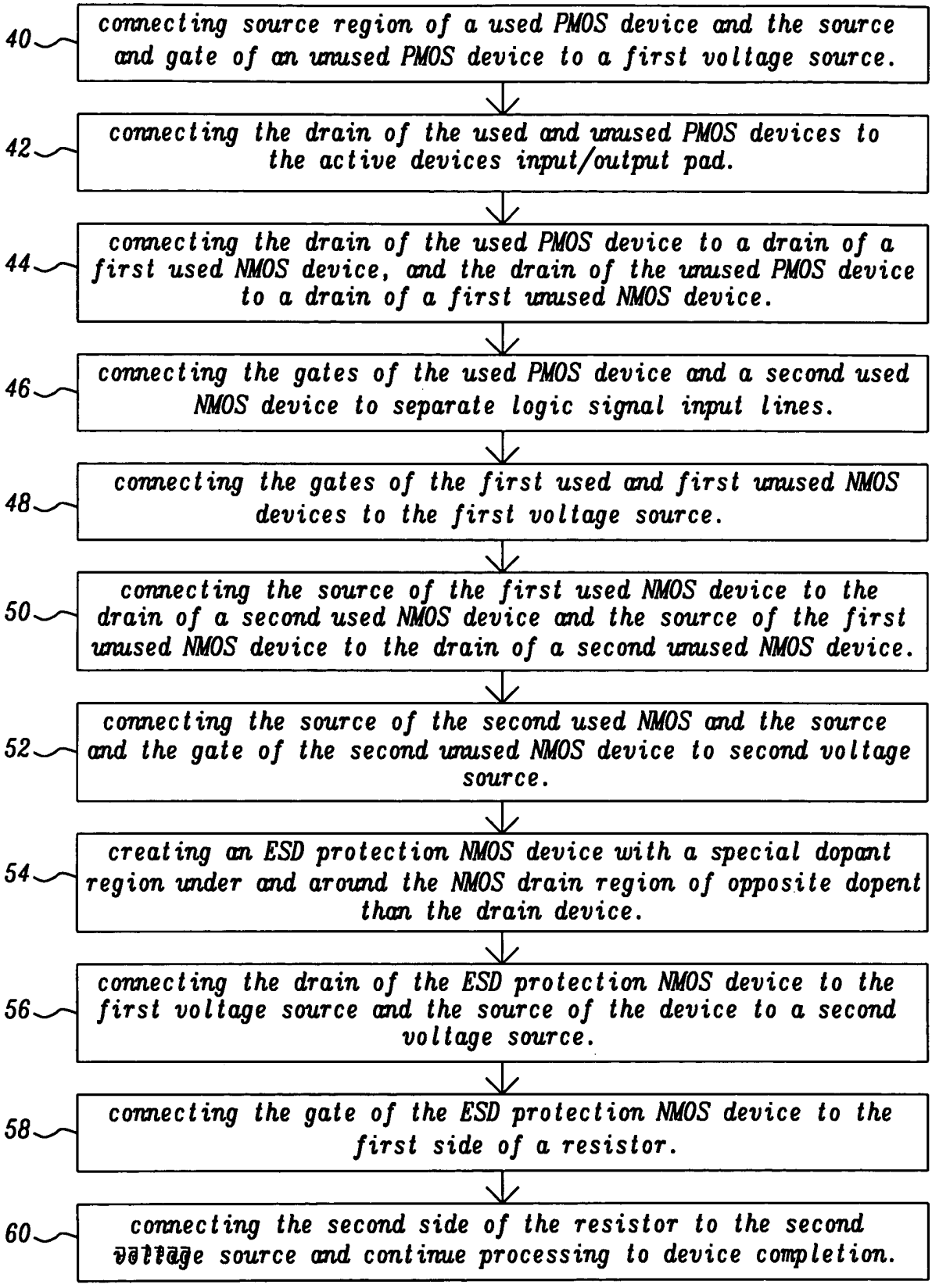

115
NP1
116
120
118
118
120
120
112
N+
N+
112
122
124
110
P-Sub
126
114
126
128

FIG. 2B


40
connecting source region of a used PMOS device and the source and gate of an unused PMOS device to a first voltage source.
42
connecting the drain of the used and unused PMOS devices to the active devices input/output pad.
44
connecting the drain of the used PMOS device to a drain of a first used NMOS device, and the drain of the unused PMOS device to a drain of a first unused NMOS device.
46
connecting the gates of the used PMOS device and a second used NMOS device to separate logic signal input lines.
48
connecting the gates of the first used and first unused NMOS devices to the first voltage source.
50
connecting the source of the first used NMOS device to the drain of a second used NMOS device and the source of the first unused NMOS device to the drain of a second unused NMOS device.
52
connecting the source of the second used NMOS and the source and the gate of the second unused NMOS device to second voltage source.
54
creating an ESD protection NMOS device with a special dopant region under and around the NMOS drain region of opposite dopent than the drain device.
56
connecting the drain of the ESD protection NMOS device to the first voltage source and the source of the device to a second voltage source.
58
connecting the gate of the ESD protection NMOS device to the first side of a resistor.
60
connecting the second side of the resistor to the second voltage source and continue processing to device completion.